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EXAMINER
MAKHDOOM, SAMARINA

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 05/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application	Applicant(s)	
	09/404,923	DOUEZY ET AL.	
	Examiner	Art Unit	
	Samarina Makhdoom	2123	

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Peri d f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-13 and 17-20* is/are rejected.

7)☒ Claim(s) *5-6 and 14-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *7 & 9* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Response to Amendment

1. Claims 1-9 are amended and claims 10-20 are newly added. Claims 1-20 are pending.

Response to Arguments

2. Applicant's arguments filed 1/05/03 have been fully considered but they are not persuasive with respect to Claims 1-4 and 7-9. See new grounds for rejection for newly added claims 10-20.

3. In the remarks, applicant argues in substance that Krakirian does not teach (1) an index to the look up table is generated by counting cycles of a base clock signal; and (2) Trimberger is not an analogous art, and thus does not cure the deficiencies of Krakirian.

4. As to arguments (1) – (2), (1) See Col. 4, lines 39 et Seq and Table I. Karkirian teaches putting the clock signals in a look up table. An index (such as row and column number) is inherent to a table. (2) In response to applicant's argument that Trimberger is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Trimberger discloses in Figure 21, a timing circuit for generating multiple internal cycles for each external clock cycle thus Trimberger is analogous to applicant's claimed invention as well as Krakirian.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 1-4 and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krakirian, U.S. Patent No. 6,064,247 in view of Trimberger, U.S. Patent No. 5,701,441.

As per Claims 1 and 8, Krakirian discloses a method for clock generation and distribution in a system comprising:

generating a derived clock signal from a look up table, wherein an index to the look up table is generated by counting cycles of a base clock signal (See Col. 4, lines 39 et Seq and Table I. The clock output and input signals are presented in Table 1 to provide a glitch-free clock. Also See Col. 2, lines 25 et Seq for the use of a counter to divide down the frequency of the input (i.e. base) clock signal for the output (derived) clock signal. Therefore the lookup table contains the binary values needed to generate the output (derived) clock signals);

Krakirian does not explicitly teach emulating the clock generating circuit, stopping the emulation, or restarting the emulation.

Trimberger discloses emulating a Field Programmable Gate Array with multiple sequencers, each sequencer allows operation with multiple user clocks. (See Col. 17, lines 21 et Seq) therefore teaching the emulation of a clock signal. Trimberger also discloses emulating an internal or external signal indicate a stop condition (See Col. 17, lines 44-56) therefore stopping the emulation. Trimberger also discloses running a sub-network that may be pre-empted (or stopped) and placed in a waiting state for resources to become available. Once the resources are available the running or emulating the sub-network is restarted (See Col. 37, lines 13 et Seq) therefore Trimberger teaches restarting the emulation.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the multiple frequency clock generation circuit of Krakirian with the emulation of Trimberger because it would allow Krakirian to emulate the clock generation circuit and evaluate it's performance before manufacturing the circuit saving both time and money.

As per Claims 2 and 9, Krakirian discloses the step of generating a derived clock further comprises:

accessing an entry in a look up table having an address corresponding to the number of intermediate clock signals that have been counted (See Col. 2, lines 25 et Seq for the use of a counter. This counter can be used for counting signals in a look up table like an index marker);

and outputting a signal level in response to the entry accessed (See Col. 4, lines 13 et Seq and Table 1. Table 1 contains the input clock signal CIN, is gated with two control signals CnH

and CnL. The output (derived) clock signal is Cn, where n is an integer multiple of the input (base) clock signal CIN).

As per Claim 3, Krakirian a clock generation circuit comprising:

a base clock generation circuit that generates a base clock signal of a first frequency, and a derived clock generation circuit having (See Col. 3, lines 45 et Seq. for the disclosure of a clock generation circuit having an apparatus to generate multiple frequency output (derived) clock signals from an input (base) clock signal),

a frequency divider circuit coupled to receive the base clock signal (See Figure 6A for a Frequency Control Module item 600. Col. 6, lines 20 et Seq. disclose that the frequency control module 600 generates multiple frequency output clock signals that are twice, three, and four times the duration of the input (base) clock signal. Therefore the clock signal frequency is divided into half, thirds, or fourths),

a counter circuit coupled to receive an output of the frequency divider circuit (See Col. 2, lines 25 et Seq for the use of a counter to divide down the frequency of the input (i.e. base) clock signal for the output (derived) clock signal), and

a look up table coupled to receive an output of the counter circuit (See Col. 4, lines 13 et Seq and Table 1 – a truth or look up table. Table 1 contains the input clock signal CIN, is gated with two control signals CnH and CnL. The output (derived) clock signal is Cn, where n is an integer multiple of the input (base) clock signal CIN),

wherein the output of the counter circuit is used to index entries in the look up table (See Col. 4, lines 13 et Seq and Table 1 – a truth or look up table. Table 1 contains the input clock

signal CIN, is gated with two control signals CnH and CnL. The output (derived) clock signal is Cn, where n is an integer multiple of the input (base) clock signal CIN),

and further wherein the entries in the look up table indicate a signal level for a derived clock signal generated by the clock generation circuitry (See Col. 4, lines 13 et Seq and Table 1. Table 1 contains the input clock signal CIN, is gated with two control signals CnH and CnL. The output (derived) clock signal is Cn, where n is an integer multiple of the input (base) clock signal CIN thereby indicating a signal level for the derived clock signal).

As per Claim 4, Krakirian discloses a plurality of clock generation circuits coupled in parallel to generate a plurality of derived clock signals (See Figure 6A, for the generation of clock signals in parallel and the corresponding text in Col. 6, lines 13 et Seq).

As per Claim 7 Krakirian does not teach emulating the clock generating circuit or the use of a multiplexor.

Trimberger discloses emulating a Field Programmable Gate Array with multiple sequencers, each sequencer allows operation with multiple user clocks. (See Col. 17, lines 21 et Seq) therefore Trimberger emulates clock signals. Trimberger also discloses micro cycle sequencing in a time-multiplexed programmable logic device. In order to time multiplex signals, a multiplexor circuit is inherent (See Col. 25, lines 60 et Seq) therefore, the reference teaches the use of a multiplexor to time multiplex signals.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the multiple frequency clock generation circuit of Krakirian with the emulation of Trimberger because it would allow Krakirian to emulate the clock generation circuit before manufacturing the circuit saving both time and money.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

6. Claims 10-13 and 17-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Karkirian, U.S. Patent No. 6,064,247.

As per Claims 10 and 19, Karkirian discloses an apparatus for generating a derived clock signal, the apparatus comprising:

a counter to count cycles in a base clock signal and to provide a counter out corresponding to a number of counted cycles (See Col. 2, lines 11-24 for a counted used to divide the input clock signal. Dividing the input clock signals requires counting the number of cycles. The output of the counter is routed through a register)

a look up table to receive the counter output as a sequence of indexes and to output a sequence of signal values from entries in the look up table that correspond to the sequence of indexes, said sequence of signal values comprising the derived clock signal (See Col. 4, lines 39 et Seq and Table I. The clock output and input signals are presented in Table 1 to provide a glitch-free clock. Also See Col. 2, lines 25 et Seq for the use of a counter to divide down the frequency of the input (i.e. base) clock signal for the output (derived) clock signal. Therefore the lookup table contains the binary values needed to generate the output (derived) clock signals);

outputting a sequence of located signal values from the look up table, said sequence of located signal values comprising the derived clock signal (See Col. 5, lines 37-53 for output clock signal C1 that is in the look up table in Col. 4, lines 45-55).

As per Claim11, Karkirian discloses the apparatus of Claim 10, wherein each entry in the look up table contains a plurality of signal values (See Col. 4, lines 39-67 for a look up table with a plurality of signal values such as Clock in, Clock High),

each of said plurality of signal values corresponding to a different one of a plurality of derived clock signals (See Col. 4, lines 39-67 for a look up table with a plurality of signal values such as Clock in, Clock High. Clock in and Clock High correspond to derived clock signals).

As per Claims12 and 18, Karkirian discloses the apparatus of Claim 10 further comprising: a frequency divider to divide a first signal down to the base signal and provide the base signal to the counter (See Figure 6A for a Frequency Control Module item 600. Col. 6, lines 20 et Seq. disclose that the frequency control module 600 generates multiple frequency output clock signals that are twice, three, and four times the duration of the input (base) clock signal. Therefore the clock signal frequency is divided into half, thirds, or fourths).

As per Claim13, Karkirian discloses the apparatus of Claim 10 further comprising: a multiplexor to receive a first signal and a second signal and to selectively provide one of the first signal and second signal to the counter as the base signal (See Figure 8, the circuit for 600 the frequency control module and text in Col. 9, line 5-24. The first clock signal C4h, and the second signal Cin (base clock) are multiplexed in to the output signal C4).

As per Claim17, Karkirian discloses the apparatus of Claim 10 wherein the counter comprises a three-bit counter, and said sequence of indexes comprises a repeated sequence from 0 to 7 (See Col. 2, line 25-34 for a counter. The number of bits are inherent to the counter).

As per Claim 20, Karkirian discloses the method of Claim 19 wherein each entry contains a plurality of additional signal values, the method further comprising:

outputting a plurality of additional sequences of located signal values from the look up table (See Col. 5, lines 37-53 for output clock signal C1 that is in the look up table in Col. 4, lines 45-55),

each of said plurality of additional sequences of located values comprising an additional derived clock signal (See Col. 5, lines 37-53 for output of a plurality of clock signals C1, C2, C3, and C4 that are derived clock signals of Cin the base clock signal. All these signals are in the look up table in Col. 4, lines 45-55).

Allowable Subject Matter

9. Claims 5-6, and 14-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samarina Makhdoom whose telephone number is 703-305-7209. The examiner can normally be reached on Part Time on Friday, and Sunday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J. Teska can be reached on 703-305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-0040 for regular communications and 703-305-0040 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

SM
March 21, 2003

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER